



Addressing

U2
 1 A
 2 B
 3 C
 6 G1
 4 G2A
 5 G2B
 SN74LS138

Y0 15
 Y1 14
 Y2 13
 Y3 12
 Y4 11
 Y5 10
 Y6 9
 Y7 7

Data 0 D0 3
 Data 1 D1 4
 Data 2 D2 7
 Data 3 D3 8
 Data 4 D4 13
 Data 5 D5 14
 Data 6 D6 17
 Data 7 D7 18

U5
 11 OC
 C
 1Q 2
 2Q 5
 3Q 6
 4Q 9
 5Q 12
 6Q 15
 7Q 16
 8Q 19
 SN74LS374

Title Output Circuit			Dan Kohn NC A&T State University
Size: A	Number:	Revision:	
Date: 27-Mar-2008	Time: 10:33:29	Sheet0 of 0	
File: C:\Documents and Settings\dekohn\My Documents\New folder\Lab_Project.ddb - Documents\Output.Sch			