Lab #7
I/O Card Part #1
Addressing

Rev Nov 20, 2007

This is the 1st part of the construction testing and programming of an 8 bit I/O card. The finished card will be demonstrated to the instructor at the end of the semester and a written report will be submitted on the theory and testing of the card.

Purpose:

To familiarize students with I/O Addressing and the ISA (Industry Standard Architecture) expansion slot.

Discussion:

In the robot arm experiment, you saw that each I/O port has its own unique address (for that experiment we were dealing with the Parallel Port Data Port at address 378H).

This week we will start to build and I/O card of our own.

The first thing an I/O card must be able to do is interpret the address to see if the signals being sent over the expansion slot are meant for our I/O Card or another card. The simplest way to do this is to use standard gates to interpret the address lines and give an active output when the card address is on the address lines (as well as a few control lines).

It must be noted that, as in the ROM experiment, the chip select ($\overline{CS}$) of the IC's we will be using to perform the I/O Functions are ACTIVE LOW. This means that the output of our circuit must be low when the correct address is on the bus, and must be high when the address is incorrect.

The first part of our circuit will use the 74LS688 (8bit comparator).

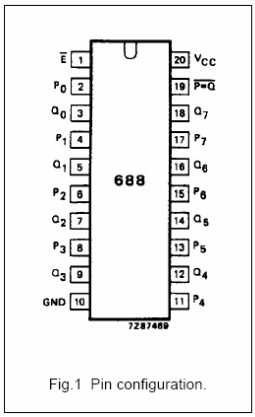


Fig.1 Pin configuration.

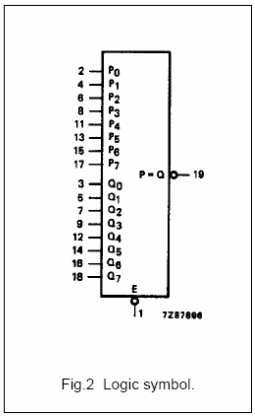


Fig.2 Logic symbol.

From: http://www.learn-c.com/74ls688.pdf

This IC compares 2 8-bit inputs (P0..P7 and Q0..Q7) and gives an ACTIVE LOW signal out when the two values are equal.

For flexibility, we will make one input selectable (using a dip switch configuration similar to that used in the ALU experiment - Switch closed = HIGH, Switch Open = LOW), so that we can change the address of the card. This is done for two reasons:

1) If there is a hardware conflict in the computer, we can change the address by simply changing the switches instead of re-wiring the card.

2) We can put more than one card in a PC with each card having a unique address.

In our case, we will wire pins A1..A8 to the P0..P7 inputs of the IC. (Two more address lines will be used: A0 and A9, but they will be inputs to another IC).

Once wired, any pattern set on the dip switch will have to be matched on the A1..A8 lines from the BUS for a LOW output to appear on the OUTPUT line (Pine 19).

One other input will be required. The $\overline{E}$ (aka $\overline{G}$) line will need to be active. For this we will use AEN

Now that we have interpreted the address lines A1..A8, we need to complete the addressing of the I/O Card. For this we will need to handle address line A0 and A9, as well as the lines that tell us the DIRECTION of the data (Input or Output, Lines IOR and IOW).

For this we will use a 74LS138 (a 3-to8 line decoder/demultiplexer; inverting):

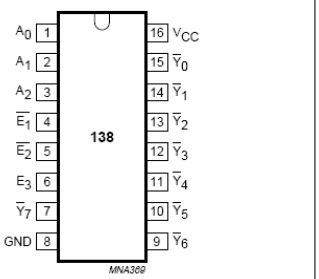


Fig.1 Pin configuration.

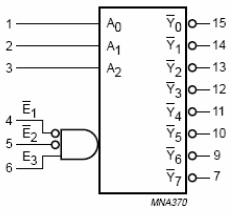


Fig.2 Logic symbol.

From: http://www.learn-c.com/74ls138.pdf

This IC will interpret the inputs on A0..A2 (aka A,B,C) and activate the corresponding output pin (Y0..Y7). For example if A2..A0 is 010_{bin} then Y2 will activate (it will go LOW, since these are ACTIVE LOW signals). All other Y lines will be inactive!

This helps us because we can then put the IOR and IOW on two of the inputs and this will individually activate various components to Read or Write data from/to the data bus.

In our case we will wire A0 to A0 (A), IOW to A1 (B) and IOR to A2 (C). To activate the IC we also must activate E1..E3 (aka G1, G2A and G2B). For these we will use +5V, the Output of the 74LS688 and A9 respectively.

Construction:

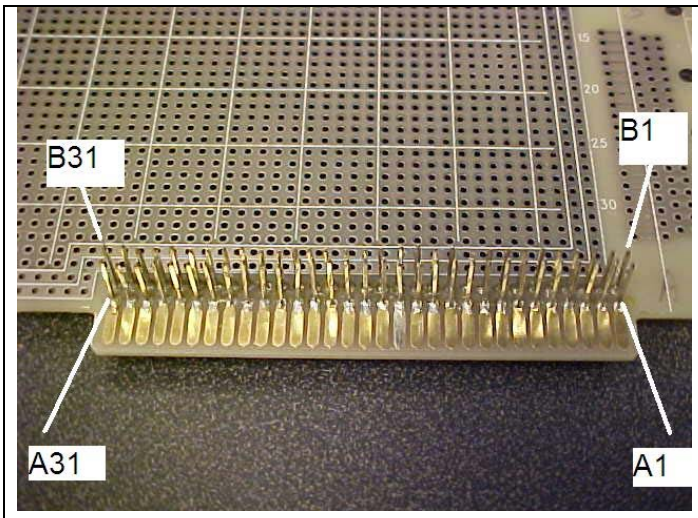
We will be using WIRE WRAPPING techniques to wire the circuit. For more info on how to wire wrap read:

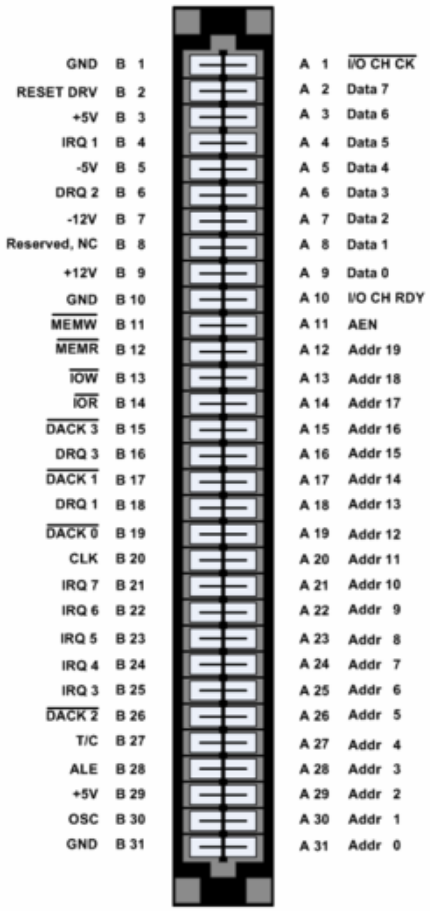
http://www.tecratools.com/pages/tecalert/wirewrap_guide.html

This technique will be demonstrated by the instructor.

The schematic for the circuit is attached to the end of the lab along with the pinout of the ISA bus. The Schematic DOES NOT show the +5V and GND connections for the IC's. To determine the power and ground connections for the 74LS688 and 74LS138, see the data sheet for the individual IC.

IMPORTANT NOTE: The schematic shows the SIGNAL NAMES, not the pin numbers of the ISA bus. **A1** is referring to **ADDRESS 1** not pin A1 on the bus.





From:
http://en.wikipedia.org/wiki/Industry_Standard_Architecture

Further information on the ISA bus is available at the link above; this is just a SUMMARY for quick reference. It is the students responsibility to understand those lines used in the I/O card, for this information will appear on tests and exams.