

**Department of  
Electronics, Computer, and Information  
Technology**

ECT 213 Digital Electronics

**Lecture 9:**

Chapter 5

Bubble Pushing

Universal Gates

Sum of Products, Product of Sum

Karnaugh Mapping (POS)

Chapter 6

X-OR gates

X-Nor gates

Parity

# Bubble Pushing

A Shortcut method of forming equivalent logic circuits that is based on De Morgan's theorem.

1. Change logic gate
  - a. AND to OR
  - b. OR to AND
2. Switch inversion bubbles
  - a. Add bubbles where there are none
  - b. Remove the original bubbles

## **Example 1: Bubble Pushing**

## Sum-of-Products (SOP) form

- two or more ANDed variables ORed  
ORed with two or more other variables  
ANDed together

$$X = A\bar{B} + AC + \bar{A}BC$$

$$X = AC\bar{D} + \bar{C}D + B$$

$$X = B\bar{C} \bullet \bar{D} + \bar{A}BDE + CD$$

## Product-of-sums (POS) form

- two or more ORed variables within ()  
ANDed with two or more other variables  
within ()

$$X = (A + \overline{B}) \bullet (B + C)$$

$$X = (B + \overline{C} + D)(BC + E)$$

$$X = (A + \overline{C})(\overline{B} + E)(C + B)$$

## Two ways to solve one K-map

	C	
AB	$\bar{C}$	$C$
$\bar{\bar{A}}\bar{B}$	1	1
$\bar{A}B$	1	
$AB$		
$\bar{A}\bar{B}$		

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## **Universal Gates**

The NAND and NOR gate are referred as Universal gates

Combinations of NAND gates can form  
An inverter, AND, OR, and NOR  
Gate.

Combinations of NOR gates can form an  
Inverter, AND, OR, and NAND gate.

**Example 2:** Use a combination of NAND gates  
To form an inverter, AND, OR, and  
Nor Gate.

## Exclusive-OR (X-OR) Gates:

A	B	X
0	0	
0	1	
1	0	
1	1	

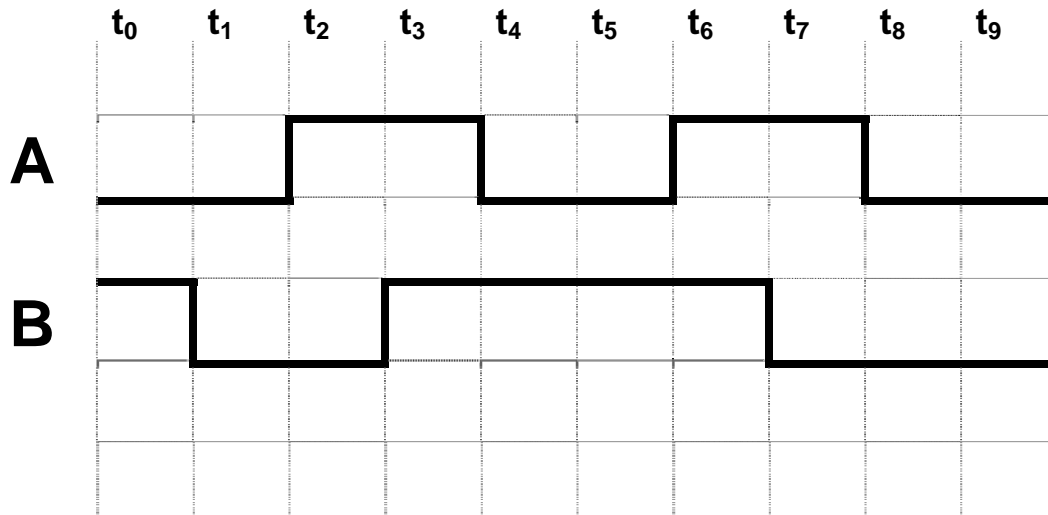
## Exclusive-NOR (X-NOR) Gates:

	A	B	X
	0	0	
	0	1	
	1	0	
	1	1	

**Example 14:**

$$X = (A \oplus B)\overline{B}$$

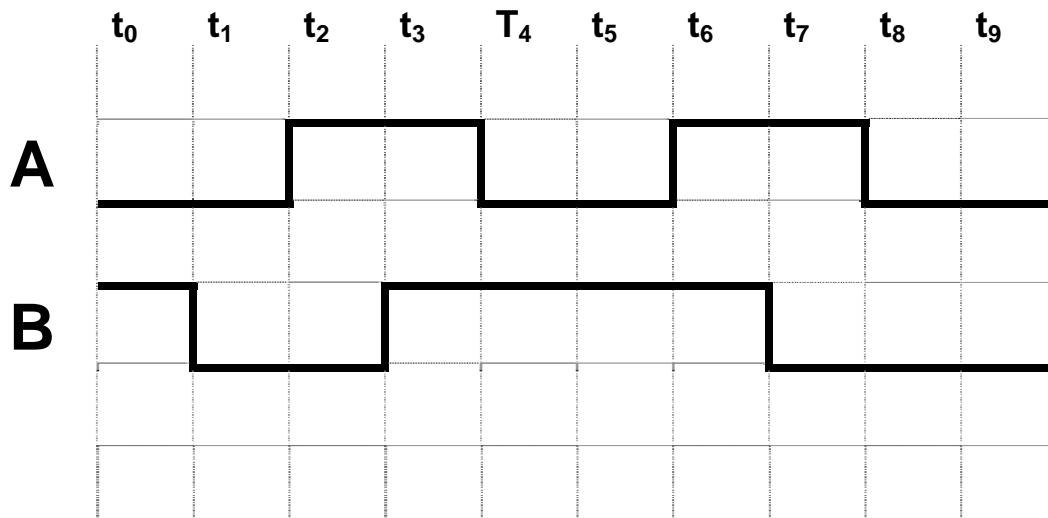
	A	B	X
	0	0	
	0	1	
	1	0	
	1	1	



### Example 15:

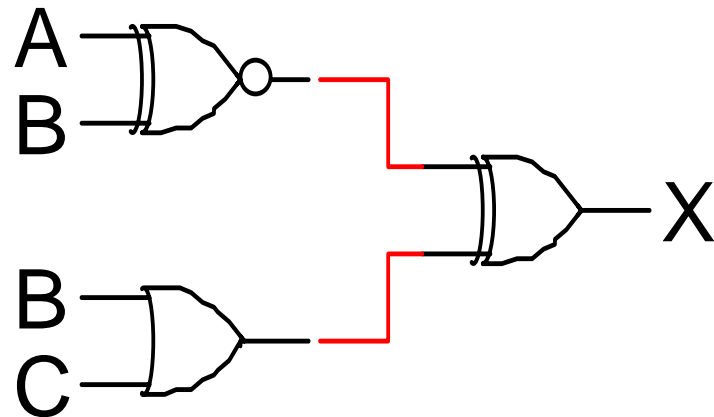
			A	B	Y
			0	0	
			0	1	
			1	0	
			1	1	

$$Y = \overline{(A \oplus B)} \overline{B}$$

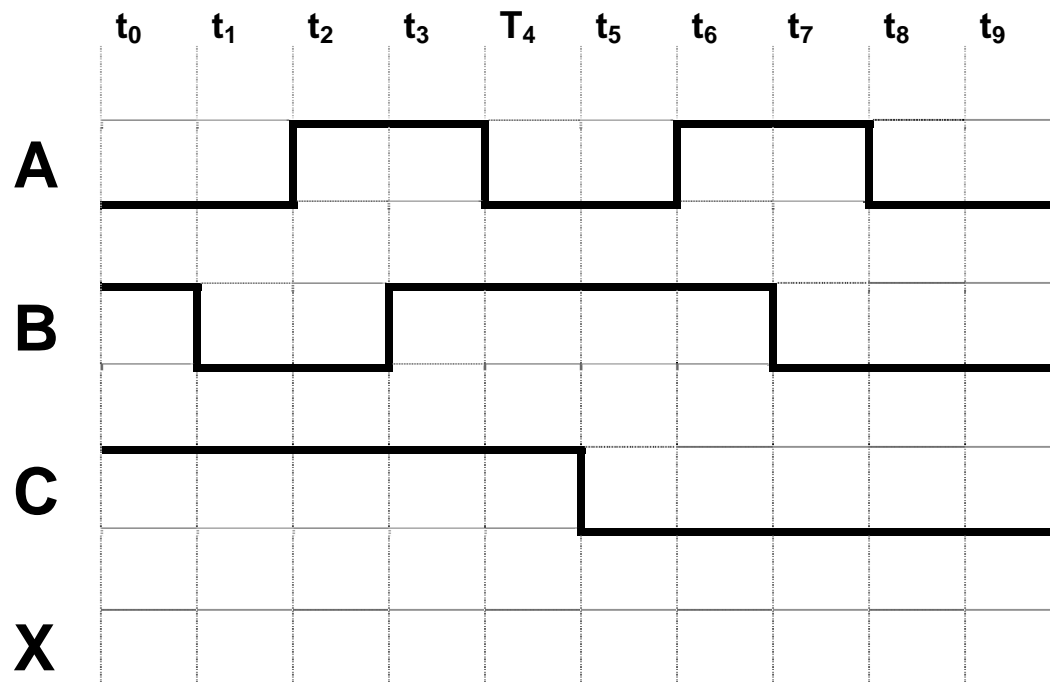


**Example 16:** Complete the Truth Table of the following circuit

			A	B	C	X
			0	0	0	
			0	0	1	
			0	1	0	
			0	1	1	
			1	0	0	
			1	0	1	
			1	1	0	
			1	1	1	



**Example 17:** Complete the timing diagram using the truth table in example 16.



# Parity

There is a possibility for electrical noise or other disturbances to cause an error in the transmission of binary information.

A method for determining if the transmitted digital data is corrupted involves counting the number of bits whose value is high. An extra bit would then be transmitted indicating the parity.

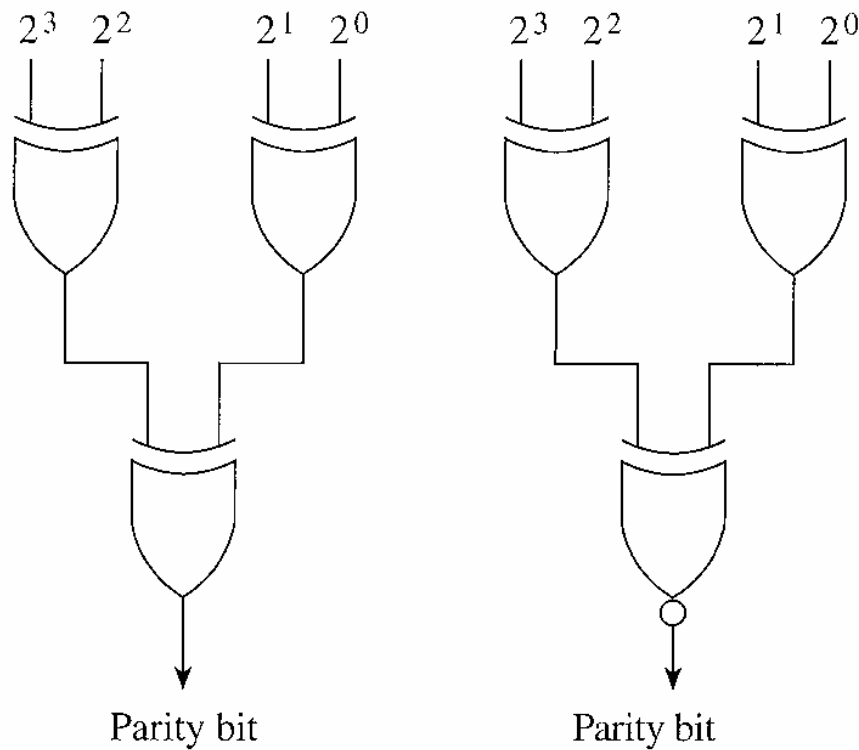
<b>Odd Parity</b>	<b>Even Parity</b>
The parity bit would be: <ul style="list-style-type: none"><li>• 1 if sum total is even</li><li>• 0 if sum total is odd</li></ul>	The parity bit would be: <ul style="list-style-type: none"><li>• 0 if sum total is even</li><li>• 1 if sum total is odd</li></ul>

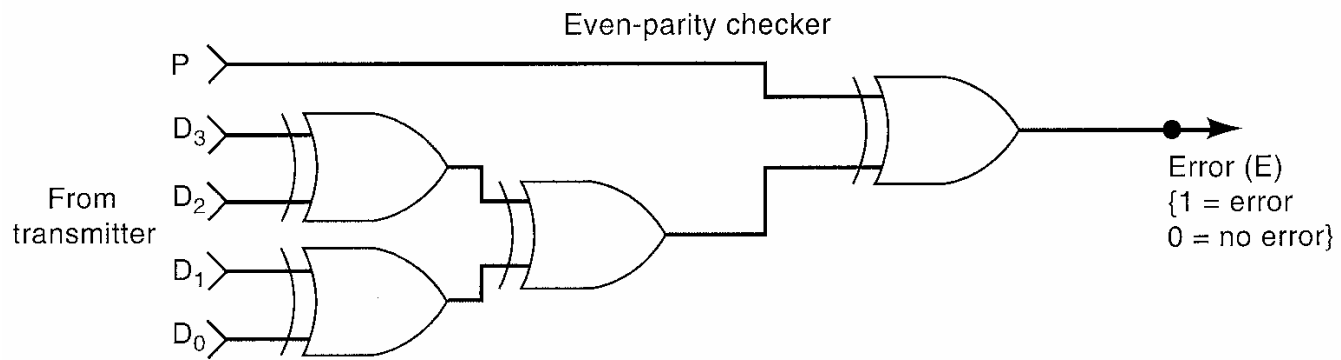
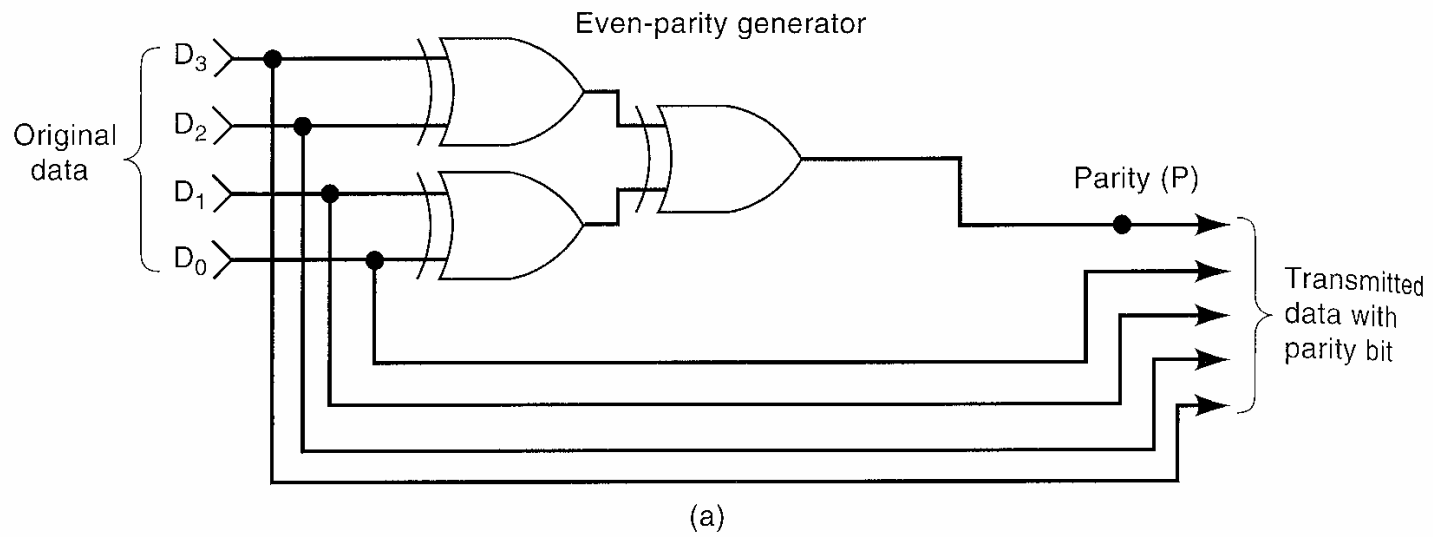
**Example 7:** Convert the following numbers to their 8-bit binary code. Add a parity bit next to the LSB to form odd parity.

	8-Bit binary code	Odd parity	Even parity
72			
$10100_2$			
$00101001_{\text{BCD}}$			
$72_8$			
$\text{EF}_{16}$			

## **Example 7: Continued**

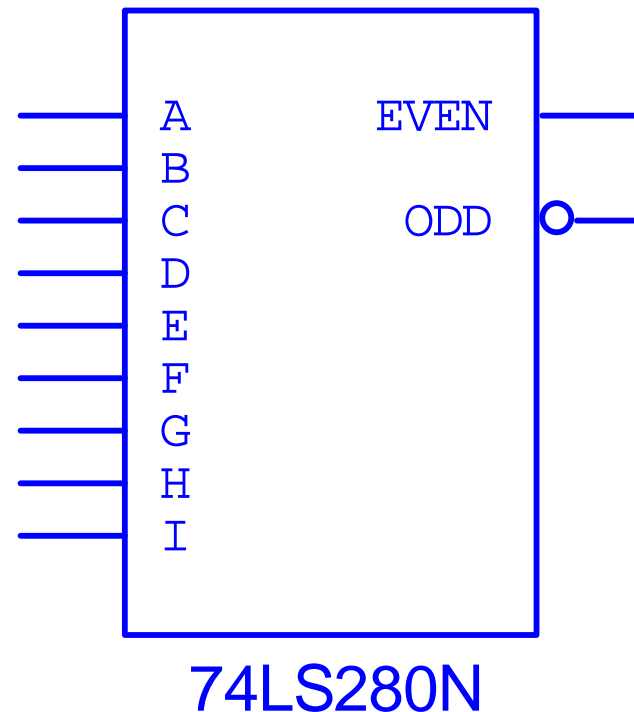
**Example 8:** Determine if the following is Even and Odd Parity generator using X-Or and X-Nor gates.



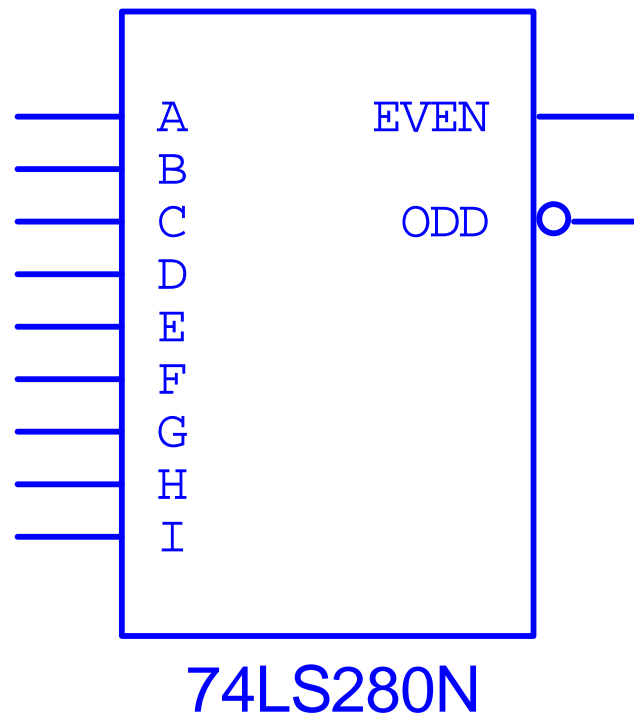


## 74280 9-bit Parity generator/checker

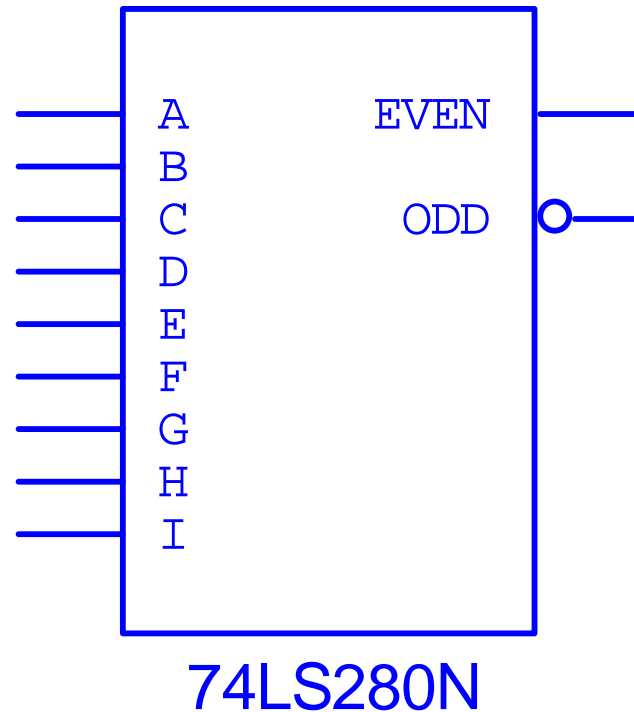
Function Table		
Number of High Data Inputs (A – I)	Output	
	Even	Odd
Even	High	Low
Odd	Low	High



**Example 9:** Design a 4-bit even-parity generator using the 74280 Chip.



**Example 10:** Design a 4-bit odd-parity generator using the 74280 Chip.



**Example 11:** Design an 8-bit odd-parity error detection system using two 74LS280 and 9-line transmission cable.

