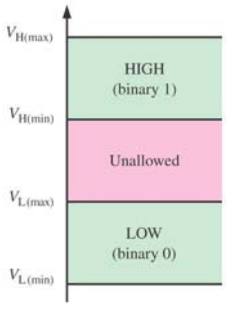
ECT 213 Digital Electronics

Lecture 2
Sections of Chp 2 / Instructor Notes / Floyd Chp 1
Digital Signals
Serial / Parallel

Digital Values

Digital: discrete levels in waveform.
High level represents On / 5v / High
Low level represents Off / 0v / Low

Figure 1–5 Logic level ranges of voltage for a digital circuit.



Manual Switches

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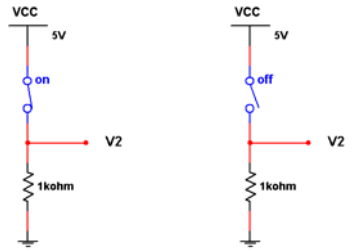
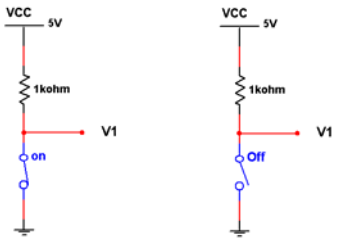
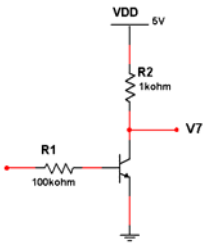


Manual Switches



Transistors as a Switch

NPN transistor



Transistors

NPN PNP

Binary Digits, Logic Levels, and Digital Waveforms

Binary values are also represented by voltage levels

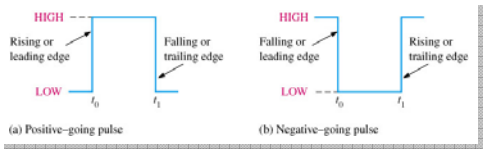


Figure 1–8 Examples of digital waveforms.

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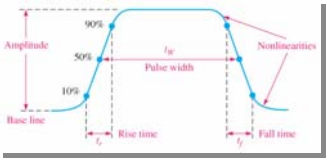
Digital Fundamentals, 9e

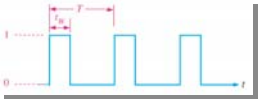
Binary Digits, Logic Levels, and Digital Waveforms

Major parts of a digital pulse

- Base line
- Amplitude
- Rise time (t_r)
- Pulse width (t_w)
- Fall time (t_f)



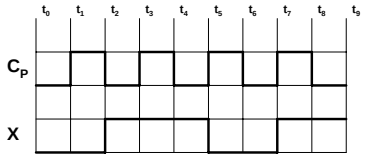
Binary Digits, Logic Levels, and Digital Waveforms



- t_w = pulse width
- T = period of the waveform
- f = frequency of the waveform

$$\mathbf{f = \frac{1}{T}}$$

Timing Diagrams



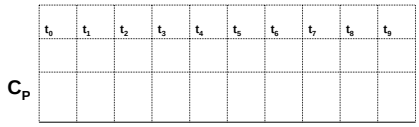
2 μs intervals

C_P: periodic clock waveform
t_p: Period of Clock:
F: Frequency

$$f = \frac{1}{t_p}$$

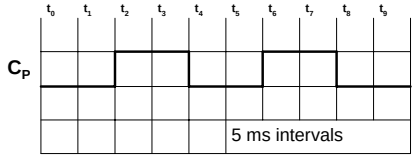
Example

Determine the period of clock waveform whose frequency is 500 kHz. Draw the clock signal and label the time divisions.



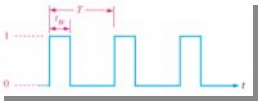
Example

Given the following timing diagram, determine the period of clock, CP, and its frequency.



TP =
F =

Binary Digits, Logic Levels, and Digital Waveforms



The duty cycle of a binary waveform is defined as:

$$\text{Duty cycle} = \left(\frac{t_W}{T}\right)100\%$$

Figure 1–10 Example of a clock waveform synchronized with a waveform representation of a sequence of bits.

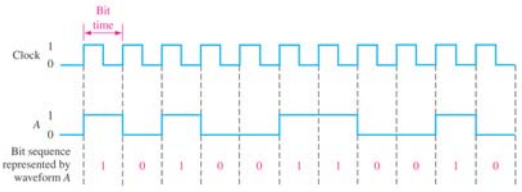
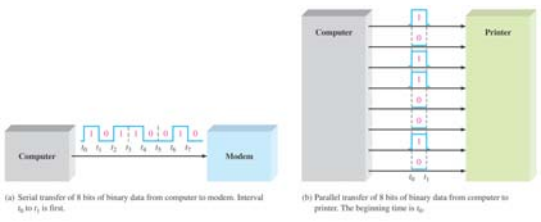


Figure 1–12 Illustration of serial and parallel transfer of binary data. Only the data lines are shown.



(a) Serial transfer of 8 bits of binary data from computer to modem. Interval t_0 to t_1 is first.

(b) Parallel transfer of 8 bits of binary data from computer to printer. The beginning time is t_0.

Digital Logic Families

Transistor/Transistor Logic (TTL) Integrated Circuit

- Most common integrated circuit
- Will be used with labs in this course
- Uses combinations of bipolar transistors in design of logic gates
- All IC's in this family start with '74' in number

CMOS

- Common integrated circuit
- Uses combinations of metal oxide semiconductor field-effect transistors (FET)
- Advantage: Low power consumption
- Disadvantage: Susceptible to electrostatic discharge
- Most IC's in this family start with '40' or have 'HC'

Digital Logic Families

- TTL and CMOS IC's cannot be directly connected to each other since each family uses different voltages for Logic 0 and Logic 1.

Equipment Used in Digital Logic

Figure 1–57 Typical DMMs. Courtesy of B+K Precision.®

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Logic Probe

Figure 1–40 A typical dual-channel oscilloscope. Used with permission from Tektronix, Inc.

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Figure 1–47 An oscilloscope voltage probe. Used with permission from Tektronix, Inc.

Figure 1–49

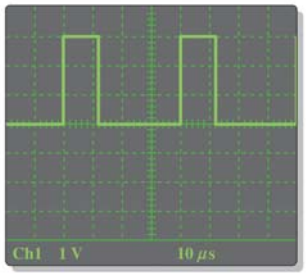


Figure 1–50 Typical logic analyzer. Used with permission from Tektronix, Inc.

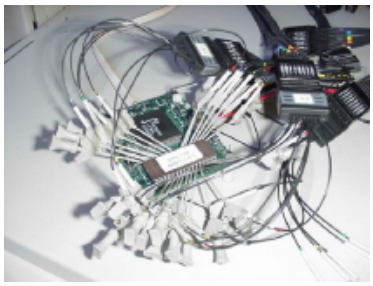
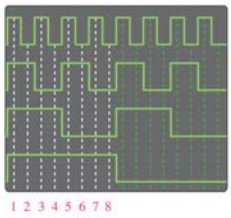


Figure 1–52 Two logic analyzer display modes.



(a) Waveform display

Sample	Binary	Hex	Time
1	1111	F	1 ns
2	1110	E	10 ns
3	1101	D	20 ns
4	1100	C	30 ns
5	1011	B	40 ns
6	1010	A	50 ns
7	1001	9	60 ns
8	1000	8	70 ns

(b) Listing display

Figure 1–54 Typical signal generators. Used with permission from Tektronix, Inc.

(a) An arbitrary waveform generator.

(b) Examples of function generators.

Working With IC's

Figure 1–27 Cutaway view of one type of fixed-function IC package showing the chip mounted inside, with connections to input and output pins.

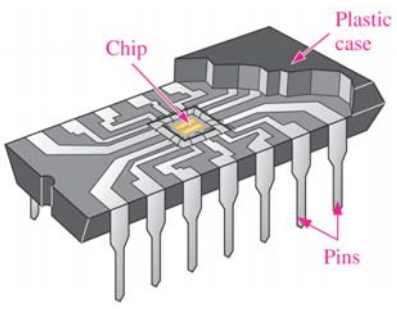


Figure 1–28 Examples of through-hole and surface-mounted devices. The DIP is larger than the SOIC with the same number of leads. This particular DIP is approximately 0.785 in. long, and the SOIC is approximately 0.385 in. long.

(a) Dual in-line package (DIP)

(b) Small-outline IC (SOIC)

Figure 1–30 Pin numbering for two standard types of IC packages. Top views are shown.

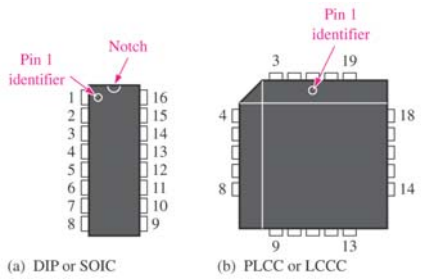
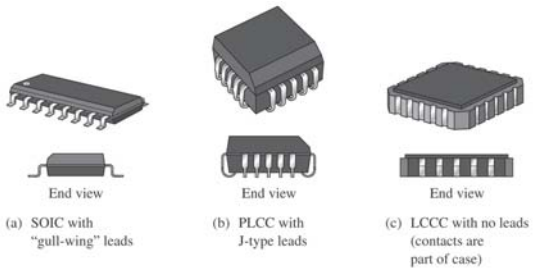


Figure 1–29 Examples of SMT package configurations.



Breadboarding

Breadboard – 1

Breadboard - 2