

ECT 213
Spring 2008
Lab #7
Adder

Name: _____

Purpose: To introduce the student to digital logic circuits that perform mathematical operations (in this case addition).

Introduction: Read about adders at <http://www.play-hookey.com/digital/adder.html>

Lab procedure: Using the knowledge obtained in the above reading, draw a 3 bit adder circuit in HADES using a half-adder circuit for the Least Significant Bit (LSB) and then two full adders for the next two bits. We will call one of the 3 bit numbers 'A' and the other number 'B'. Since A and B are 3 bits each, we will call the LSB A0 and B0, the next bit A1 and B1 and the Most Significant Bit (MSB) A2 and B2.

eg: add 4 + 7 (100b + 111b)

<pre style="margin: 0;"> 1 0 0 + 1 1 1 ----- 1 0 1 1 b </pre>	<pre style="margin: 0;"> A₂ A₁ A₀ + B₂ B₁ B₀ ----- S₃ S₂ S₁ S₀ </pre>
---	---

Simulate the circuit and fill in the truth table below:

B _{dec}	A _{dec}	B ₂	B ₁	B ₀	A ₂	A ₁	A ₀	S _{dec}	S ₃	S ₂	S ₁	S ₀
0	0	0	0	0	0	0	0					
0	1	0	0	0	0	0	1					
0	2	0	0	0	0	1	0					
0	3	0	0	0	0	1	1					
0	4	0	0	0	1	0	0					
0	5	0	0	0	1	0	1					
0	6	0	0	0	1	1	0					
0	7	0	0	0	1	1	1					
1	0	0	0	1	0	0	0					
1	1	0	0	1	0	0	1					
1	2	0	0	1	0	1	0					
1	3	0	0	1	0	1	1					

1	4	0	0	1	1	0	0					
1	5	0	0	1	1	0	1					
1	6	0	0	1	1	1	0					
1	7	0	0	1	1	1	1					
2	0	0	1	0	0	0	0					
2	1	0	1	0	0	0	1					
2	2	0	1	0	0	1	0					
2	3	0	1	0	0	1	1					
2	4	0	1	0	1	0	0					
2	5	0	1	0	1	0	1					
2	6	0	1	0	1	1	0					
2	7	0	1	0	1	1	1					
3	0	0	1	1	0	0	0					
3	1	0	1	1	0	0	1					
3	2	0	1	1	0	1	0					
3	3	0	1	1	0	1	1					
3	4	0	1	1	1	0	0					
3	5	0	1	1	1	0	1					
3	6	0	1	1	1	1	0					
3	7	0	1	1	1	1	1					
4	0	1	0	0	0	0	0					
4	1	1	0	0	0	0	1					
4	2	1	0	0	0	1	0					
4	3	1	0	0	0	1	1					
4	4	1	0	0	1	0	0					
4	5	1	0	0	1	0	1					
4	6	1	0	0	1	1	0					
4	7	1	0	0	1	1	1					
5	0	1	0	1	0	0	0					
5	1	1	0	1	0	0	1					
5	2	1	0	1	0	1	0					
5	3	1	0	1	0	1	1					
5	4	1	0	1	1	0	0					
5	5	1	0	1	1	0	1					
5	6	1	0	1	1	1	0					
5	7	1	0	1	1	1	1					
6	0	1	1	0	0	0	0					
6	1	1	1	0	0	0	1					
6	2	1	1	0	0	1	0					
6	3	1	1	0	0	1	1					
6	4	1	1	0	1	0	0					
6	5	1	1	0	1	0	1					
6	6	1	1	0	1	1	0					
6	7	1	1	0	1	1	1					
7	0	1	1	1	0	0	0					

7	1	1	1	1	0	0	1						
7	2	1	1	1	0	1	0						
7	3	1	1	1	0	1	1						
7	4	1	1	1	1	0	0						
7	5	1	1	1	1	0	1						
7	6	1	1	1	1	1	0						
7	7	1	1	1	1	1	1						

Submit the Hades simulation as “Lab 7 – Adder CCT” via online submission.

Print out a copy of the simulation, **label the IC’s and pin numbers** for each gate on the printout.

Build the circuit following your schematic.

Demonstrate the circuit to the instructor for credit:

instructors initials here

Questions: 1) What is the difference between a half and full adder?

2) In the half adder, what does the AND gate do?

